PILLSBURY WINTHROP SHAW PITTMAN LLP
DAVID A. JAKOPIN (S.B. No. SBN 209950)
david.jakopin@pillsburylaw.com
2475 Hanover Street
Palo Alto, CA 94304
Phone: (650) 233-4500
Fax: (650) 233-4545

RICHARD H. ZAITLEN (S.B. No. 063283)
richard.zaitlen@pillsburylaw.com
CAROLYN S. LU (S.B. No. 233825)
carolyn.lu@pillsburylaw.com
725 South Figueroa Street, Suite 2800
Los Angeles, California 90017-5406
Telephone: (213) 488-7100
Facsimile: (213) 629-1033

Attorneys for Plaintiff
INPHI CORPORATION

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

WESTERN DIVISION

INPHI CORPORATION,
A Delaware Corporation,

Plaintiff,

vs.

NETLIST, INC., A Delaware Corporation,

Defendant.

CV09-8749 RGWL (CWx)

Case No. _____

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff Inphi Corporation ("Inphi") by and through their attorneys, Pillsbury Winthrop Shaw Pittman LLP, demands a jury trial on all issues and alleges as follows:

INTRODUCTION

This Complaint is based upon Defendant Netlist, Inc.'s ("Netlist") unauthorized making, using, selling, importing, offering to sell, and inducing others to make, use, and sell in the United States and abroad products that infringe United States Patent Nos. 7,307,863 ("the '863 Patent") and 7,479,799 ("the '799 Patent").

THE PARTIES

1. Inphi is a corporation organized and existing under the laws of the state of Delaware, authorized to do business in the state of California, with its principal place of business at 2393 Townsgate, Suite 101, Westlake Village, California 91361.

2. Inphi is informed and believes, and based thereon alleges, that Netlist is now, and at all times herein mentioned was, a corporation organized and existing under the laws of the state of Delaware, authorized to do business in the state of California, with its principal place of business at 51 Discovery, Irvine, California 92618.

JURISDICTION

3. This action for patent infringement arises under, among other things, the United States Patent Laws, 35 U.S.C. § 101, et seq. Subject matter jurisdiction is therefore based upon 28 U.S.C. §§ 1331 and 1338(a), providing for federal question jurisdiction of patent infringement actions and exclusive jurisdiction of patent infringement actions in the U.S. district courts.

4. Personal jurisdiction is proper over Netlist because Netlist has purposefully availed itself of the laws of the State of California by selling,

offering for sale, importing, and inducing others to make, use, and sell throughout California and in this judicial district, products that infringe the '863 and '799 patents.

VENUE

5. Inphi is informed and believes, and thereon alleges, that this Court is the appropriate venue for this matter pursuant to 28 U.S.C. §§ 1391(b)-(d) and 1400(b) because the acts of patent infringement alleged herein were engaged in within this judicial district.

FACTS

6. Inphi is a private high-speed analog semiconductor company that provides critical enabling components for telecommunications, networking, computer servers and storage equipment, and is dedicated to the innovative design and manufacturing of components that operate at critical memory interfaces. Inphi's research, development and marketing of its memory interface products allow Inphi to service markets including manufacturers of memory modules for high end computer servers used in data centers.

7. Inphi's memory interface products are designed for a wide range of applications. These applications include enterprise servers, data center servers, high performance computer systems, telecommunications network equipment, supercomputers, storage area networks, and others. Inphi has been manufacturing and selling memory interface products since 2004.

8. On December 11, 2007, the United States Patent and Trademark Office duly and lawfully issued United States Patent No. US 7,307,863 (the '863 Patent), titled "Programmable Strength Output Buffer For RDIMM Address Register." A true and correct copy of the '863 Patent is attached hereto as Exhibit "A".

9. On January 20, 2009, the United States Patent and Trademark Office duly and lawfully issued United States Patent No. US 7,479,799 (the '799 Patent), titled "Output Buffer With Switchable Output Impedance." A true and correct copy of the '799 Patent is attached hereto as Exhibit "B".

10. Inphi is the current owner of all rights, title and interest in the '863 and '799 Patents.

11. Inphi is informed and believes, and based thereon alleges, that Netlist designs, manufactures, uses, sells, offers to sell and/or markets memory products that incorporate the Inphi technology claimed in the '863 and '799 Patents. Such infringing memory products include, without limitation, Netlist's DDR3 Memory Modules, including the DDR3 memory modules referred to as HyperCloud Memory.

12. A copy of the website product page for Netlist DDR3 RDIMM memory modules is attached as Exhibit "C".

13. A copy of a Datasheet of the HyperCloud Memory is attached as Exhibit "D".

14. Inphi is informed and believes, and thereon alleges, that with knowledge of and in direct contravention of Inphi's rights to the '863 and '799 Patents, Netlist is and has been infringing, contributing to the infringement of, and inducing others to infringe one or more claims of the '863 and '799 Patents through the unauthorized manufacture, use, sale and offering for sale of memory products, including those comprising the DDR3 Memory Modules and the HyperCloud Memory, throughout the United States, including in this judicial district. Additionally, Inphi is informed and believes, and thereon alleges, that Netlist has in the past and still is infringing, contributing to the infringement of and inducing others to infringe the '863 and '799 Patents by the unauthorized sale and offer for sale of memory products to, among others,

Original Equipment Manufacturers (OEMs) in the United States, including in this judicial district.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 7,307,863

(35 U.S.C. § 271)

15. Inphi repeats, realleges, and incorporates by reference, as though fully set forth herein, the allegations set forth in paragraphs 1 through 14.

16. Netlist has directly and contributorily infringed, and has induced others to infringe, at least one or more claims of the '863 Patent by the unauthorized manufacture, use, offering to sell and/or sale of infringing products within the United States, including this judicial district.

17. On information and belief, Netlist is and has been willfully infringing one or more claims of the '863 Patent.

18. As a result of Netlist's infringement of the '863 Patent, Inphi has and is suffering irreparable harm for which Inphi has no adequate remedy at law. Unless enjoined by this Court, Netlist's infringement of the '863 Patent will continue and will result in further irreparable harm to Inphi.

19. Inphi is entitled to recover damages from Netlist adequate to compensate for the infringement.

SECOND CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 7,479,799

(35 U.S.C. § 271)

20. Inphi repeats, realleges, and incorporates by reference, as though fully set forth herein, the allegations set forth in paragraphs 1 through 19.

21. Netlist has directly and contributorily infringed, and has induced others to infringe, at least one or more claims of the '799 Patent by the

unauthorized manufacture, use, offering to sell and/or sale of infringing products within the United States, including this judicial district.

22. On information and belief, Netlist is and has been willfully infringing one or more claims of the '799 Patent.

23. As a result of Netlist's infringement of the '799 Patent, Inphi has and is suffering irreparable harm for which Inphi has no adequate remedy at law. Unless enjoined by this Court, Netlist's infringement of the '799 Patent will continue and will result in further irreparable harm to Inphi.

24. Inphi is entitled to recover damages from Netlist adequate to compensate for the infringement.

PRAYER FOR RELIEF

WHEREFORE, Inphi prays for relief and judgment from this Court:

(a) For an order declaring that the '863 and '799 Patents owned by Inphi were duly and legally issued and are valid and enforceable;

(b) For a judgment declaring that Netlist has directly infringed, contributorily infringed, and/or induced the infringement of one or more claims of either the '863 Patent and/or the '799 Patent in violation of 35 U.S.C. § 271;

(c) For a judgment declaring that Netlist has willfully infringed one or more claims of either the '863 Patent and/or the '799 Patent;

(d) For an order, pursuant to 35 U.S.C. § 283, preliminarily and permanently enjoining Netlist, its officers, directors, employees, successors and assigns, agents, attorneys, subsidiaries, parent corporations, and all persons in active concert with Netlist as follows:

1. from selling or offering for sale any product falling within the scope of the claims of the '863 Patent and/or the '799 Patent;

2. from importing any product into the United States which falls within the scope of the claims of the '863 Patent and/or the '799 Patent;

3. from manufacturing any product falling within the scope of the claims of the '863 Patent and/or the '799 Patent;

4. from using any product or method falling within the scope of any of the claims of the '863 Patent and/or the '799 Patent;

5. from inducing others to infringe any claims of the '863 Patent and/or the '799 Patent;

6. from engaging in acts constituting contributory infringement of any of the claims of the '863 Patent and/or the '799 Patent; and

7. from all other acts of infringement of any of the claims of the '863 Patent and/or the '799 Patent;

(e) That Netlist be required to prepare and deliver to the Court, or to such agents as the Court may designate, a complete list of entities to whom Netlist distributed or sold products that infringe the '863 and/or the '799 Patents and that Netlist be required to serve a copy of such list on Inphi's attorneys;

(f) For an award of damages, together with prejudgment interest, to compensate Inphi for Netlist's infringement of the '863 and '799 Patents, such damages being trebled pursuant to 35 U.S.C. § 284 for the willful, wanton, and deliberate nature of such infringement;

(g) For costs and reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

(h) For a judgment declaring this to be an exceptional case; and

(i) For such other and further relief as this Court deems proper and just.

DATED: November 30, 2009

Respectfully Submitted,

DAVID A. JAKOPIN
RICHARD H. ZAITLEN
CAROLYN S. LU
PILLSBURY WINTHROP SHAW PITTMAN LLP

By: _____
Richard H. Zaitlen
Attorneys for Plaintiff
INPHI CORPORATION

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b), Inphi hereby demands a jury trial of all claims against Defendants.

DATED: November 30, 2009

Respectfully Submitted,

DAVID A. JAKOPIN
RICHARD H. ZAITLEN
CAROLYN S. LU
PILLSBURY WINTHROP SHAW PITTMAN LLP

By: _____
Richard H. Zaitlen
Attorneys for Plaintiff
INPHI CORPORATION

EXHIBIT A

(12) **United States Patent**
Yen et al.

(10) **Patent No.: US 7,307,863 B2**
(45) **Date of Patent: Dec. 11, 2007**

(54) **PROGRAMMABLE STRENGTH OUTPUT BUFFER FOR RDIMM ADDRESS REGISTER**

(75) Inventors: **Jeffrey C. Yen**, Camarillo, CA (US); **Nikhil K. Srivastava**, Woodland Hills, CA (US); **Gopal Raghavan**, Thousand Oaks, CA (US)

(73) Assignee: **Inphi Corporation**, Westlake Village, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 242 days.

(21) Appl. No.: **11/195,910**

(22) Filed: **Aug. 2, 2005**

(65) **Prior Publication Data**

US 2007/0030752 A1 Feb. 8, 2007

(51) **Int. Cl.**
G11C 7/00 (2006.01)

(52) **U.S. Cl.** **365/63**; 365/189.05

(58) **Field of Classification Search** 365/63, 365/189.05
See application file for complete search history.

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Dabral, S. and Maloney, T. J., *Basic ESD and I/O Design*, New York, John Wiley & Sons, Inc., pp. 162-165, 1998.

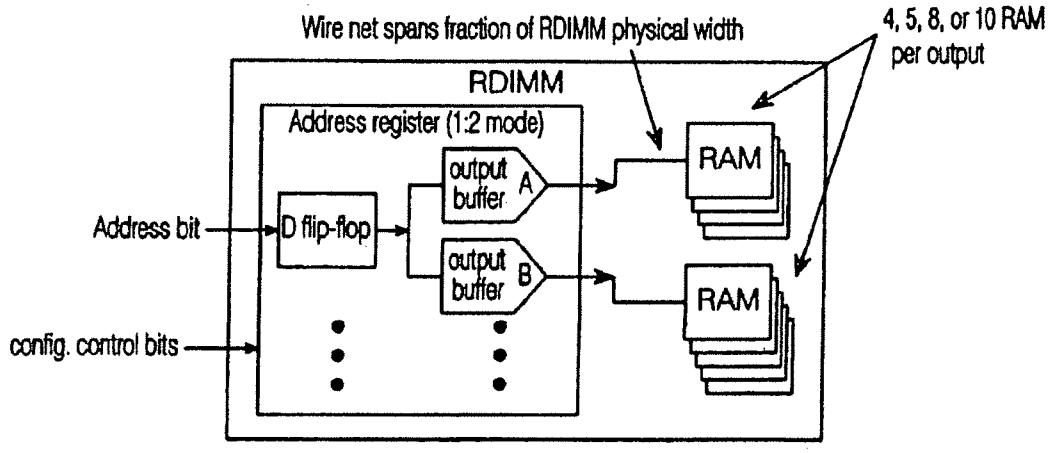
(Continued)

Primary Examiner—Michael T Tran
(74) *Attorney, Agent, or Firm*—Koppel, Patrick, Heybl & Dawson

(57) **ABSTRACT**

A programmable strength output buffer intended for use within the address register of a memory module such as a registered DIMM (RDIMM). The output signals of an array of such buffers drive respective output lines that are connected to the address or control pins of several RAM chips. The programmable buffers vary the strength of at least some of the output signals in response to a configuration control signal, such that the output signals can be optimized for the loads to which they will be connected.

16 Claims, 5 Drawing Sheets



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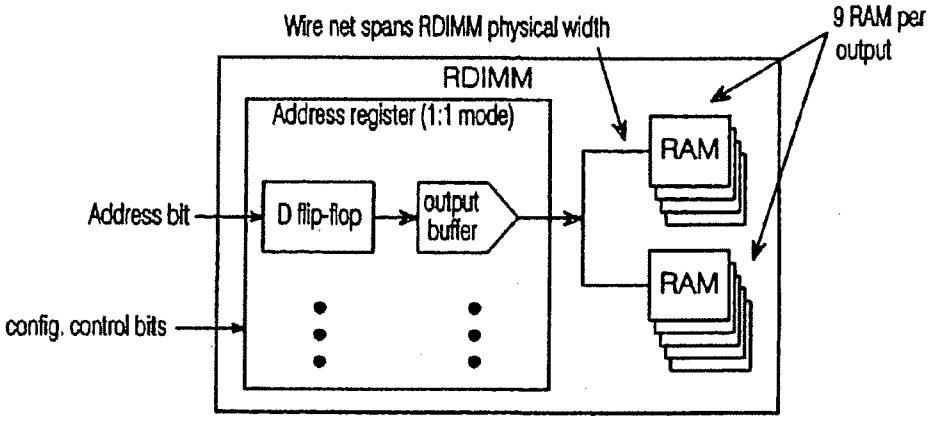

Wire net spans RDIMM physical width
9 RAM per output
RDIMM
Address register (1:1 mode)
Address bit
D flip-flop
output buffer
config. control bits
RAM
RAM

FIG.1a

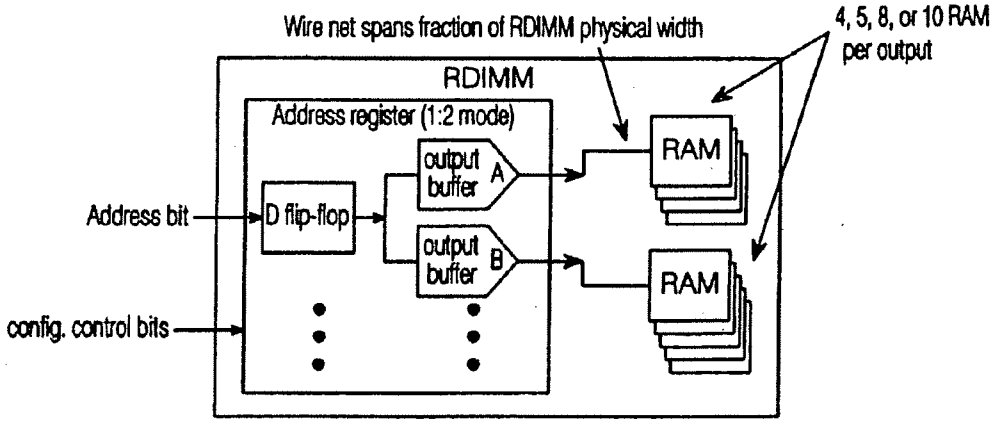

Wire net spans fraction of RDIMM physical width
4, 5, 8, or 10 RAM per output
RDIMM
Address register (1:2 mode)
Address bit
D flip-flop
output buffer A
output buffer B
config. control bits
RAM
RAM

FIG.1b

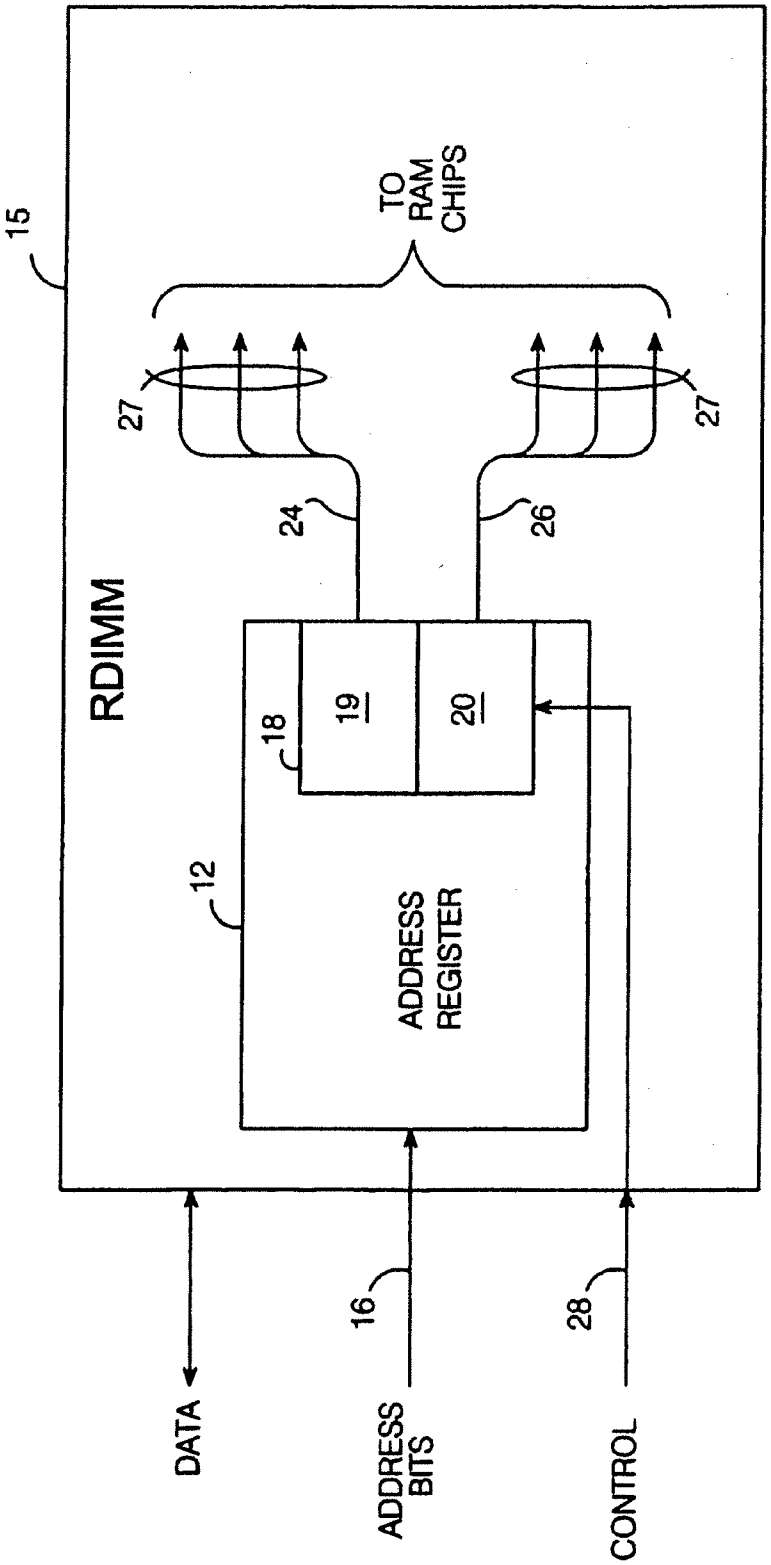

15
TO RAM CHIPS
27
27
24
26
RDIMM
18
19
20
12
ADDRESS REGISTER
16
28
DATA
ADDRESS BITS
CONTROL

FIG.2

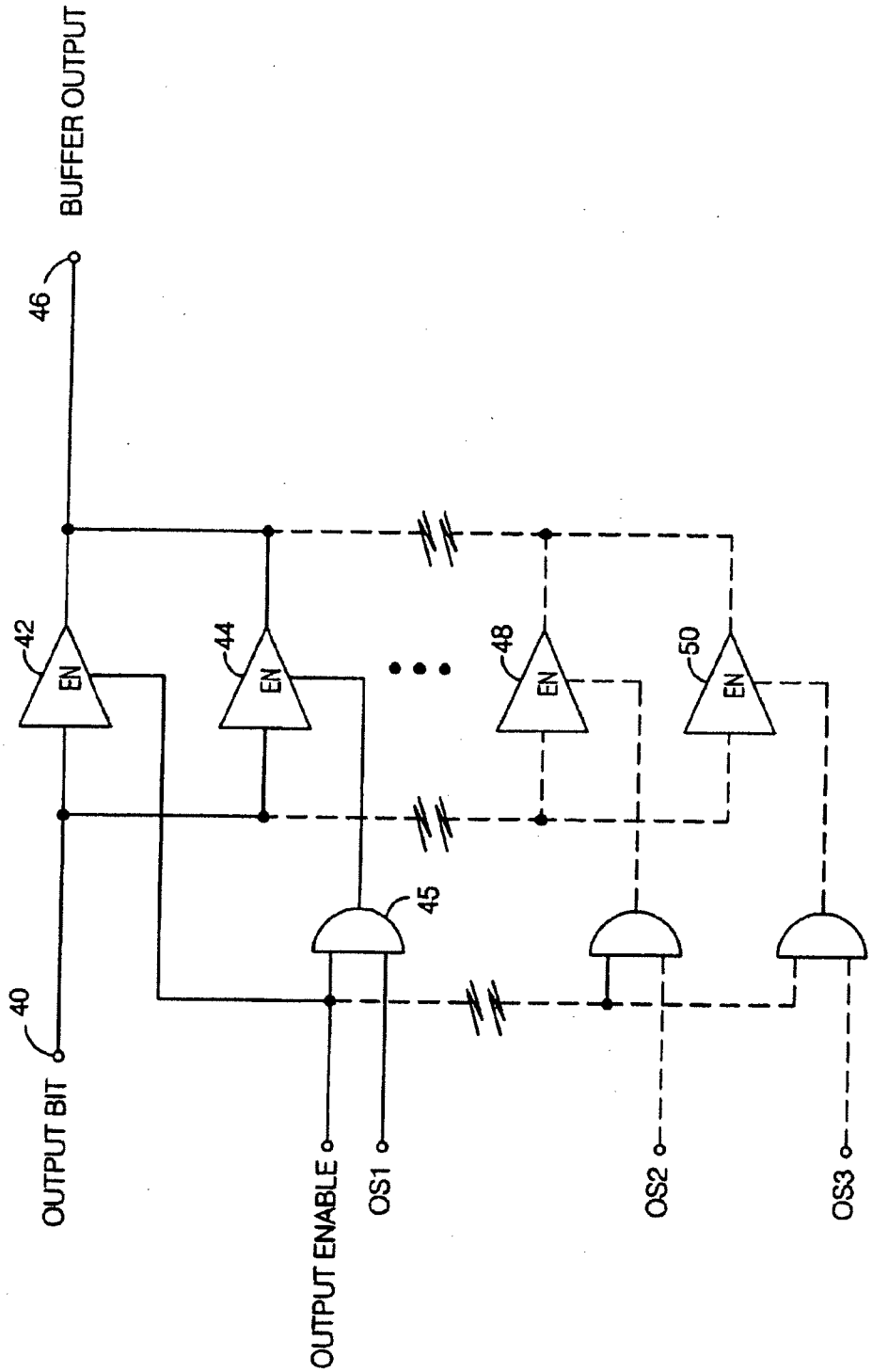

BUFFER OUTPUT
46
42
44
48
50
EN
EN
EN
EN
45
40
OUTPUT BIT
OUTPUT ENABLE
OS1
OS2
OS3

FIG.3

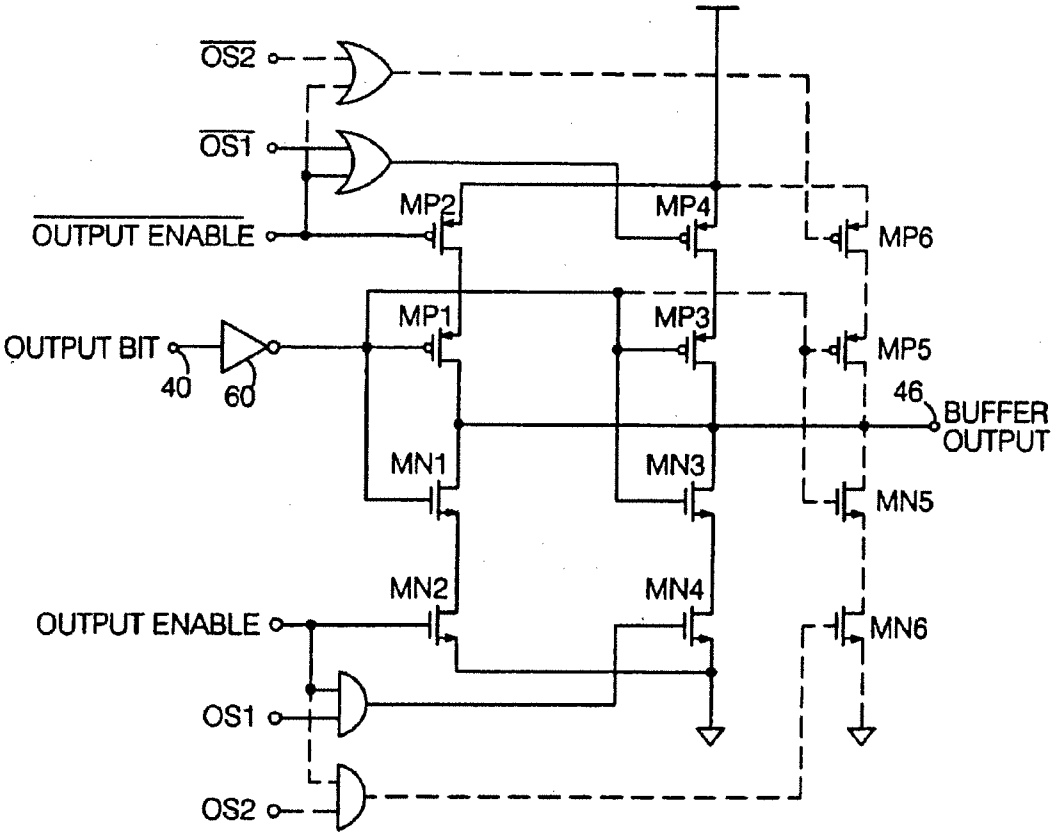
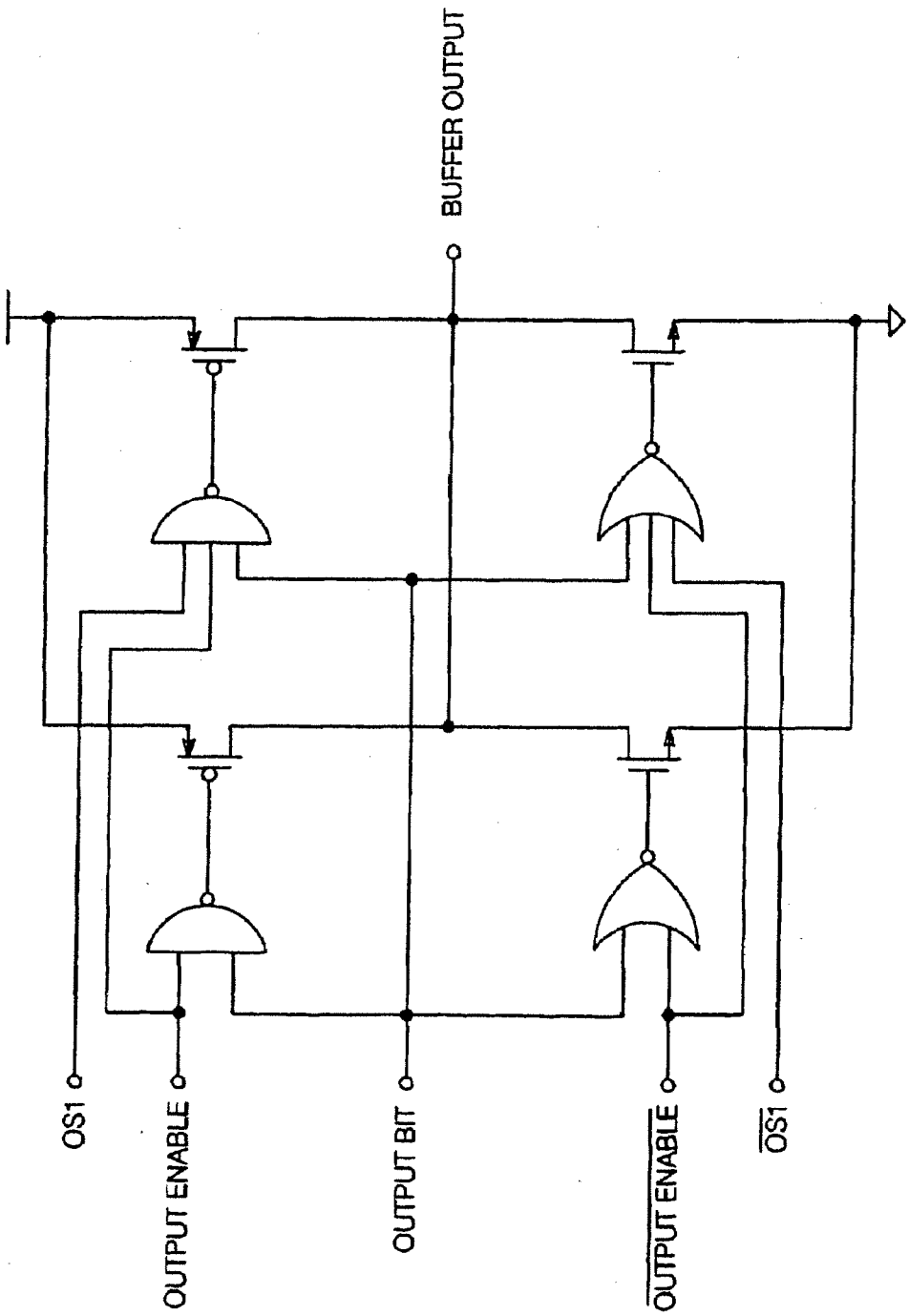

OS2
OS1
OUTPUT ENABLE
MP2
MP4
MP6
MP1
MP3
MP5
OUTPUT BIT
40
60
46
BUFFER OUTPUT
MN1
MN3
MN5
MN2
MN4
MN6
OUTPUT ENABLE
OS1
OS2

FIG.4

FIG.5


BUFFER OUTPUT
OS1
OUTPUT ENABLE
OUTPUT BIT
OUTPUT ENABLE
$\overline{OS1}$

PROGRAMMABLE STRENGTH OUTPUT BUFFER FOR RDIMM ADDRESS REGISTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of memory modules, and particularly to the output buffers of Registered Dual-Inline Memory Module (RDIMM) address registers.

2. Description of the Related Art

Dual-Inline Memory Modules (DIMMs) are the industry-standard platform on which random access memory (RAM) is provided for digital computers. Each DIMM is a printed-circuit board that contains a number of individual RAM integrated circuits (ICs) or "chips." One variety of DIMM, called a registered DIMM (RDIMM), contains an address register that acts as an electrical buffer, distributing received memory address bits to each of the RDIMM RAM chips. RDIMMs are provided in a variety of configurations, each of which is referred to as a "raw card". Each raw card type, as well as RAM chip and address register component, has an associated set of specifications, promulgated by the industry-supported JEDEC Solid State Technology Association international standards body. A multitude of raw card configurations exist due to the need to support different RDIMM memory capacities, as well as to support RAM chips with different internal designs, as driven by proprietary expedients that may be unique to a RAM manufacturer or manufacturing process.

One JEDEC specification details an address register that may be used on several different raw cards. One raw card type contains 9 RAM chips whose address pins are wired together in a network spanning the physical width of the RDIMM; an exemplary embodiment is shown in FIG. 1*a*. The other raw card types contain 18 RAM chips that are subdivided according to their placement on the RDIMM. Depending upon the logical functionality of each address bit, the address pins of the RAM chips may be wired together in groups of 4, 5, 8, or 10, in wiring networks spanning only half the physical width of the RDIMM; an exemplary embodiment of this RDIMM configuration is shown in FIG. 1*b*.

To support these different raw card configurations, the address register contains an array of 28 output buffers and 28 corresponding output pins that may be organized in one of two ways. A configuration control bit applied to the address register selects between the two array deployments. As shown in FIG. 1*a*, the array may be organized as a 1:1 fanout array, in which 25 address bits applied as inputs are distributed to 25 of the 28 output buffers (only one buffer is shown) in 1:1 correspondence. This arrangement is specified for the raw card configuration of 9 DRAM chips wired together. Alternately, as shown in FIG. 1*b*, the array may be organized as a 1:2 fanout array. In this case, the array is split into two sub-arrays of 14 output buffers, denoted "A" and "B" (only two buffers are shown), with 14 address bits applied as inputs fanning out to 28 output pins through both the A and B sub-arrays. This arrangement is specified for any of the raw cards containing 18 DRAM chips, in order to support the divided wiring arrangement of the 18 chips. In order to support the 25-28 address bits required for JEDEC-standard DDR2 RDIMMs, two registers are used on an RDIMM when using registers in 1:2 fanout mode. A second configuration control bit is used to distinguish the two registers according to the specific DRAMs to which they are wired.

Conventionally, the output buffers have a unique fixed output "strength": each buffer produces a characteristic output current and transient slew rate when driving a standardized electrical load. The output strength is engineered ad hoc for either a specific raw card configuration, or an electrical approximation that represents the mathematical average of relevant electrical dimensions of all the possible raw card configurations for which the register is intended. Address register output signal integrity degrades when the number of DRAM input pins, and/or the dimension of the wire network driven by an output buffer, differs from that for which it was designed. Signal integrity degradation can take the form of ringing, overshoot, and/or pulse reflections, all of which reduce system reliability, and impose limits on operating speed as the frequency-dependence of the actual output load amplifies the electrical loading at higher operating speed.

SUMMARY OF THE INVENTION

A programmable strength output buffer is presented which overcomes the reduced system reliability and operating speed limits noted above, by enabling the strength of the output buffers of an RDIMM address register to be varied as needed for a particular raw card application.

The present programmable strength output buffer is intended for use with memory modules that include a signal repeater which drives output lines, the loading of which depends on the particular module configuration. A primary application of the invention is an RDIMM having an address register which includes an array of the present programmable strength output buffers, with the output signals provided by the buffers driving respective output lines that are connected to the address or control pins of several RAM chips. The register is arranged to receive a configuration control signal which, in one embodiment, indicates the type of raw card on which the address register resides, and varies the strength of at least some of the register's output signals in response to the configuration control signal. In this way, the strength of the output buffer signals can be optimized for the loads to which they will be connected on the indicated raw card type, thereby reducing the signal integrity degradations that might otherwise occur.

The configuration control signal may take a variety of forms, depending upon the degree of flexibility of configuration and configuration programmability desired. Conformant to JEDEC specification, there may be two configuration control bits hardwired to logic levels on the RDIMM; alternately, there may be a greater number of configuration control bits hardwired on the RDIMM, making use of redundant register pins to complete the connection to the output buffers. Also, any number of configuration control bits may be stored (and also re-programmed) in a re-writable memory storage device, such as an EEPROM residing on the RDIMM, using the JEDEC-specified pins as well as redundant register pins as necessary. Further, any number of configuration control bits may be driven by the memory subsystem, linking to the address register through JEDEC-specified and redundant register pins and through redundant lines on the connector between the RDIMM and memory subsystem.

An output buffer in accordance with the present invention could be arranged such that the strength of each of the register's output buffers is programmed to be equal in response to the configuration control signal. Alternately, different subsets of output buffers could be set to respective strengths in response to the configuration control signal, or

each output buffer could be individually programmed to a desired strength in response to the configuration control signal.

Further features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1***a* and **1***b* depict known RDIMM configurations.

FIG. **2** is a block diagram illustrating the basic principles of a programmable strength output buffer per the present invention.

FIG. **3** is a block/schematic diagram of a programmable strength output buffer per the present invention.

FIG. **4** is a schematic diagram of a programmable strength output buffer per the present invention.

FIG. **5** is a schematic diagram of another possible implementation of a programmable strength output buffer per the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present programmable strength output buffer is generally applicable for use with memory modules that include a signal repeater which drives output lines, the loading of which depends on the particular module configuration. The signal repeater contains an array of the present programmable strength output buffers, each of which provides a respective output signal. Each programmable buffer is arranged to receive a configuration control signal, and to vary the strength of its output signal in response to the configuration control signal.

A primary application of the present invention is an RDIMM having an address register which includes a plurality of the present programmable strength output buffers, with the output signals provided by the buffers driving respective output lines that are connected to the address or control pins of several RAM chips. For purposes of illustration, this application is described throughout, though the invention is in no way limited to use with RDIMMs.

The basic principles of a programmable strength output buffer in accordance with the present invention are illustrated in FIG. **2**. Though the invention is applicable to memory modules in general (as discussed above), FIG. **2** depicts the invention in an address register **12** contained within an RDIMM raw card **15**. Address register **12** conveys a number of incoming address bits **16** to each of the RDIMM's RAM chips (not shown) via an array of programmable strength output buffers **18**; two buffers (**19**, **20**) are shown in FIG. **2**, though as noted above, an RDIMM's address register typically contains an array of **28** output buffers.

Each output buffer drives a respective output line (**24**,**26**) which is connected to an address or control pin on several RAM chips through a complex wire network **27**. As described above, the loading, comprised of several RAM chips and a complex wire network which may span the full physical width of the RDIMM, or a much smaller fraction thereof, experienced by each output signal can vary depending on the raw card type. Since the loading varies significantly, with broad variations in number of connected RAM chips and dimension of the wire network, an output signal which is not tailored for the specific load may exhibit unwanted ringing, overshoot, and/or reflections which degrade the address register output signal, reducing system reliability or imposing limits on output signal frequency.

The invention overcomes these problems by making at least some of the output buffers of array **18** programmable. Each programmable strength output buffer is arranged to receive a configuration control signal, and to vary the strength of at least some dimension of its output drive strength in response to the configuration control signal. In this way, the characteristics of the address register's output signals can be varied as needed to properly accommodate the loading presented by the raw card on which the address register is installed, thereby minimizing signal degradation.

The output signal of each buffer has an associated output current which drives its respective output line. As used herein, varying the "strength" of an output buffer comprises varying the magnitude and/or the transient slew rate of its output current.

The present output buffer is responsive to a configuration control signal. As noted above, the configuration control signal may take a variety of forms, depending upon the degree of flexibility of configuration and configuration programmability desired for a particular application; the configuration control signal is represented as a signal **28** in FIG. **2**. Conformant to JEDEC specification, the address register has two configuration control bits which may be hardwired to logic levels on the RDIMM; alternately, there may be a greater number of configuration control bits hardwired on the RDIMM, making use of redundant register pins to complete the connection to the output buffers. Also, any number of configuration control bits may be stored (and also re-programmed) in a re-writable memory storage device, such as an EEPROM residing on the RDIMM, using the JEDEC-specified pins as well as redundant register pins as necessary. Further, any number of configuration control bits may be driven by the memory subsystem, linking to the address register through JEDEC-specified and redundant register pins and through redundant lines on the connector between the RDIMM and memory subsystem. A programmable output buffer array **18** in accordance with the present invention can be arranged to receive the configuration control signal and to vary the strengths of one or more output buffers in response, to accommodate the loading presented by the indicated card's configuration of RAM chips and wiring network.

An array of programmable output buffers as described herein could be arranged such that the strength of each of the array's output buffers is programmed to the same value in response to the configuration control signal. This might be sufficient if each output signal were loaded identically.

Alternately, the buffers could be arranged such that the strength of each output buffer is individually programmed to a desired strength in response to the configuration control signal. Here, the configuration control signal would need to convey information sufficient to adjust each output buffer to the desired strength.

In yet another configuration, the output buffer array could be arranged such that subsets of output buffers are programmed to respective strengths in response to the configuration control signal. For example, in some applications, some output buffers may drive respective address lines, while other output buffers drive control lines. A control line may be lightly loaded in comparison with an address line. To accommodate this condition, the output buffers driving control lines could be set to one strength value, and the output buffers driving address lines could be set to a different strength value.

When so arranged, the programmable output buffers enable the address register on which the buffers reside to be used on a number of different raw cards, as well as with non-standard raw card designs. Each of these possible uses may present different output load characteristics, which can now be accommodated as needed to avoid the signal degradation that might otherwise occur.

An exemplary embodiment of an individual programmable output buffer, responsible for generating one output signal on the RDIMM, is shown in FIG. 3. Assuming that the output buffer is arrayed in the address register such that each of the address register output signals is programmable, circuitry such as that shown in FIG. **3** would be replicated n times for each of the address register's n output signals.

An address register output bit **40** to be provided as an output signal to one or more RAM chips is provided to the inputs of a first output driver **42** and a second output driver **44**. The outputs of drivers **42** and **44** are connected together to provide the buffer's final, programmed output signal **46**. An output strength control bit OS1 for setting the output strength of output signal **46** is derived from a configuration control signal having one of the forms discussed above; e.g., as configuration control bits hardwired to logic levels on the RDIMM, or as a signal value which has been electrically programmed into a memory storage device.

The output buffer would also typically receive an "output enable" signal. This signal is commonly employed in general memory module applications because the buffer's output signal may be driving a bi-directional bus, in which case the driver must support a non-active, high-impedance output state; or a lower-power "sleep" state; or when another driver on the same signal bus is active.

In the RDIMM address register as defined by JEDEC, output enable is not used, and is instead treated as a perpetual logic high signal.

The "output enable" signal is provided to the "enable" input of driver **42**, and the "output enable" and OS1 signals are logically combined—here, with an AND gate **45**—to provide the enable signal to driver **44**. In operation, when control bit OS1 is low, the strength of output signal **46** is determined entirely by driver **42**. However, when OS1 is high, output signal **46** is provided by both drivers **42** and **44**. Thus, for this example, output strength control bit OS1 sets buffer output signal **46** to one of two possible output strengths.

Additional resolution for setting the buffer's output strength is obtained by providing additional drivers, such as drivers **48** and **50** shown in FIG. **3**. Each additional driver is enabled in the same manner as driver **44**; i.e., with an enable signal determined by "output enable" and the state of an output strength control bit (OS2, OS3). The strengths provided by the various drivers can be arranged in any number of ways. For example, the strengths of the driver outputs could all be equal, or they could be weighted by scaling corresponding to the control bit weighting—such as binary-weighted or thermometer code-weighted. For instance, if a 2:1 dynamic range is desired for the output buffer signal, with 4 possible settings (e.g., 1.0, 1.33, 1.67, and 2.0 times minimum strength), two base-2 power-weighted output strength control bits could be employed, along with three drivers having output strength ratios of 3:2:1. For example, the ratio of the output strengths of driver **42** to driver **44** would be 3:2, and the ratio of the output strengths of driver **44** to driver **48** would be 2:1. The MSB (OS1) would control the enabling of driver **44**, and the LSB (OS2) would control the enabling of driver **48**. The arrangement shown in FIG. **3** would be replicated for each of the address register's output signals.

As noted above, an address register per the present invention could be arranged such that the strengths of each of the register's output buffers are programmed to the same strength in response to the control signal. For this case, the output strength control bits provided to each programmable strength output buffer in the address register would be the same.

Alternately, the address register could be arranged such that the strength of each output buffer is individually programmed. The address register would be arranged to provide a unique set of output strength control bits to each output buffer, as needed to achieve the desired output drive strength for each output buffer.

The output buffer could also be arranged such that subsets of output buffers are programmed to respective strengths in response to the configuration control signal. Here, the individual output buffers making up each subset would receive the same output strength control bits, with different subsets receiving different configuration control bits.

One possible implementation of a programmable strength output buffer is shown in FIG. **4**. The output bit **40** to be provided as an output signal is applied to the input of an inverter **60**, the output of which drives a PMOS FET MP1 and an NMOS FET MN1. When "output enable" is high, FETs MP2 and MN2, which are connected in series with MP1 and MN1, respectively, are turned on. When output bit **40** is high, MP1 is turned on, and MP1 and MP2 conduct current to make buffer output signal **46** high. When output bit **40** is low, MN1 is turned on, and MN1 and MN2 conduct current to pull buffer output signal **46** low.

To vary the strength of the output signal, the circuit includes a second branch of FETs which are activated when OS1 is high. The output of inverter **60** is applied to a PMOS FET MP3 and an NMOS FET MN3. When "output enable" and OS1 are high, FETs MP4 and MN4, which are connected in series with MP3 and MN3, respectively, are turned on. When output bit **40** is high, MP3 is turned on, and MP3 and MP4 conduct current to buffer output signal **46** in parallel with MP1 and MP2, thereby increasing the positive output current of signal **46**. When output bit **40** is low, MN3 is turned on, and MN3 and MN4 conduct current to buffer output signal **46** low in parallel with MN1 and MN2, thereby increasing the negative output current of signal **46**.

The programmable strength output buffer could be implemented in many different ways, and arranged to vary a number of different output signal parameters in addition to or instead of output current magnitude. For example, the circuitry could be arranged to vary the slew rate of the signal's output current in response to one or more output strength control bits.

As discussed above, the arrangement shown in FIG. **4** would be replicated for each of the address register output bits. Additional resolution for the output strength of signal **46** is obtained by providing additional drivers: in FIG. **4**, this could be achieved with another set of FETs MP5, MP6, MN5, MN6, connected to source or sink current for output signal **46** in response to a control bit OS2. The device sizes of the circuit's FETs could be sized as needed to provide a desired scaling or weighting.

Note that, though the schematics contained herein depict the use of field-effect transistors (FETs), bipolar transistors or other state-of-the-art current switching integrated circuit devices could also be used.

Another possible embodiment of a programmable strength output buffer is shown in FIG. **5**. The circuit of FIG. **4** is susceptible to a large transient short-circuit current, which can occur during the brief interval during which both PMOS and NMOS FETs conduct, as the PMOS FETs turn on and the NMOS FETs turn off, or vice-versa. As this can result in elevated power dissipation and power/ground bounce, this short circuit current may be undesirable. Short circuit current is significantly reduced for the circuit of FIG. **5**. As above, the arrangement shown in FIG. **5** would be replicated for each of the output buffer bits. Additional resolution would be achieved by adding additional branches which are responsive to additional output strength control bits.

While particular embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

We claim:

1. A Registered Dual-Inline Memory Module (RDIMM), comprising:

an address register, said register providing a plurality of output signals which drive respective output lines, at least some of which are connected to the address or control inputs of respective random-access memory (RAM) chips residing on said RDIMM;

a configuration control signal; and

an array of programmable strength output buffers within said register which provide respective ones of said output signals, said buffers arranged to receive said configuration control signal and to vary the strength of their respective output signals in response to said configuration control signal;

wherein said address register includes at least one input for receiving said configuration control signal and said at least one input on said address register comprises JEDEC-specified configuration control bits which are hardwired to logic levels on said RDIMM.

2. The RDIMM of claim **1**, wherein said at least one input further comprises additional configuration control bits which are hardwired to logic levels on said RDIMM via redundant address register pins.

3. A Registered Dual-Inline Memory Module (RDIMM), comprising:

an address register, said register providing a plurality of output signals which drive respective output lines, at least some of which are connected to the address or control inputs of respective random-access memory (RAN) chips residing on said RDIMM;

a configuration control signal; and

an array of programmable strength output buffers within said register which provide respective ones of said output signals, said buffers arranged to receive said configuration control signal and to vary the strength of their respective output signals in response to said configuration control signal;

wherein said configuration control signal is electrically programmed into a memory device that resides on said RDIMM and is provided to said address register via said address register's JEDEC-specified configuration control bits.

4. The RDIMM of claim **3**, wherein said configuration control signal is further provided to said address register via redundant address register pins.

5. A Registered Dual-Inline Memory Module (RDIMM), comprising:

an address register, said register providing a plurality of output signals which drive respective output lines, at least some of which are connected to the address or control inputs of respective random-access memory (RAM) chips residing on said RDIMM;

a configuration control signal; and

an array of programmable strength output buffers within said register which provide respective ones of said output signals, said buffers arranged to receive said configuration control signal and to vary the strength of their respective output signals in response to said configuration control signal;

wherein said configuration control signal is provided by the memory subsystem, and transmitted to said address register via said address register's JEDEC-specified configuration control bits.

6. The RDIMM of claim **5**, wherein said configuration control signal is further provided to said address register via redundant address register pins, and in turn to said redundant address register pins through redundant RDIMM connector pins.

7. A Registered Dual-Inline Memory Module (RDIMM), comprising:

an address register, said register providing a plurality of output signals which drive respective output lines, at least some of which are connected to the address or control inputs of respective random-access memory (RAM) chips residing on said RDIMM;

a configuration control signal; and

an array of programmable strength output buffers within said register which provide respective ones of said output signals, said buffers arranged to receive said configuration control signal and to vary the strength of their respective output signals in response to said configuration control signal;

wherein said address register is configurable for use with different raw cards in response to said configuration control signal.

8. A Registered Dual-Inline Memory Module (RDIMM), comprising:

an address register, said register providing a plurality of output signals which drive respective output lines, at least some of which are connected to the address or control inputs of respective random-access memory (RAM) chips residing on said RDIMM;

a configuration control signal; and

an array of programmable strength output buffers within said register which provide respective ones of said output signals, said buffers arranged to receive said configuration control signal and to vary the strength of their respective output signals in response to said configuration control signal;

wherein said programmable strength output buffers are arranged such that subsets of said output buffers are programmed to respective strengths in response to said configuration control signal.

9. A Registered Dual-Inline Memory Module (RDIMM), comprising:

an address register, said register providing a plurality of output signals which drive respective output lines, at least some of which are connected to the address or control inputs of respective random-access memory (RAM) chips residing on said RDIMM;

a configuration control signal; and

an array of programmable strength output buffers within said register which provide respective ones of said output signals, said buffers arranged to receive said

configuration control signal and to vary the strength of their respective output signals in response to said configuration control signal;

wherein said programmable strength output buffers comprises a first output driver and at least one additional output driver, the outputs of which are summed to provide said buffer's output signal, said additional output drivers enabled and disabled in response to said configuration control signal.

10. The RDIMM of claim **9**, wherein the output of each of said output drivers has an associated output current such that the output current of a programmable strength output buffer's output signal is varied in response to said configuration control signal.

11. The RDTMM of claim **9**, wherein said configuration control signal comprises a plurality of output strength control bits, said additional output drivers enabled and disabled in response to a respective one of said output strength control bits.

12. The RDIMM of claim **11**, wherein each of said programmable strength output buffers receives a respective enable signal and each of said output drivers has an enable input and is enabled and disabled in response to a signal applied to said enable input, said buffer's first output driver enabled and disabled in response to said enable signal and said buffer's additional output drivers enabled and disabled in response to a logical combination of said enable signal and a respective one of said output strength control bits.

13. The RDIMM of claim **9**, wherein said configuration control signal comprises a plurality of output strength control bits and said output drivers are enabled and disabled in response to a respective one of said output strength control bits, said RDIMM arranged such that each of said programmable strength output buffers receives the same output strength control bits such that the strengths of the output signals provided by each of said buffers is approximately equal.

14. The RDIMM of claim **9**, wherein said configuration control signal comprises a plurality of output strength control bits and said output drivers are enabled and disabled in response to a respective one of said output strength control bits, said output buffers arranged such that each of said programmable strength output buffers receives different output strength control bits such that the strengths of the output signals provided by said buffers are individually programmable.

15. The RDIMM of claim **9**, wherein said configuration control signal comprises a plurality of output strength control bits and said output drivers are enabled and disabled in response to a respective one of said output strength control bits, said programmable strength output buffers grouped into subsets each of which receive different output strength control bits, the buffers of each subset receiving the same output strength control bits such that the strengths of the output signals provided by the buffers of said subset are approximately equal.

16. A registered DIMM (RDIMM), comprising:

an address register, said register providing a plurality of output signals which drive respective output lines, at least some of which are connected to the address or control inputs of respective random-access memory (RAM) chips residing on said DIMM;

a plurality of configuration control signals;

an array of programmable strength output buffers within said register which provide said output signals, said buffers and configuration control signals arranged such that subsets of said register's output signals are programmed to respective strengths in response to said configuration control signals.

* * * * *

EXHIBIT B

US007479799B2

(12) **United States Patent**
Raghavan et al.

(10) **Patent No.: US 7,479,799 B2**
(45) **Date of Patent: Jan. 20, 2009**

(54) **OUTPUT BUFFER WITH SWITCHABLE OUTPUT IMPEDANCE**

(75) Inventors: **Gopal Raghavan**, Thousand Oaks, CA (US); **Dhruv Jain**, Woodland Hills, CA (US)

(73) Assignee: **Inphi Corporation**, Westlake Village, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 29 days.

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(51) **Int. Cl.**
H03K 19/003 (2006.01)

(52) **U.S. Cl.** **326/30**; 326/86; 326/83; 326/113

(58) **Field of Classification Search** 326/30, 326/86, 113; 327/108
See application file for complete search history.

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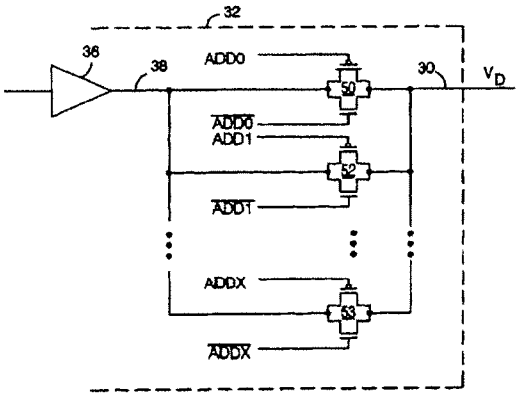
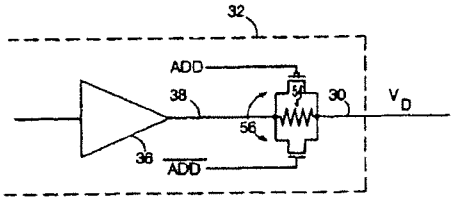
Primary Examiner—Vibol Tan
(74) *Attorney, Agent, or Firm*—Koppel, Patrick, Heybl & Dawson

(57) **ABSTRACT**

An output buffer with a switchable output impedance designed for driving a terminated signal line. The buffer includes a drive circuit, and a means for switching the output impedance of the drive circuit between a first, relatively low output impedance when the output buffer is operated in a 'normal' mode, and a second output impedance which is greater than the first output impedance when operated in a 'standby' mode. By increasing the drive circuit's output impedance while in 'standby' mode, power dissipation due to the termination resistor is reduced. When used in a memory system, additional power savings may be realized by arranging the buffer such that the increased impedance in 'standby' mode shifts the signal line voltage so as to avoid the voltage range over which a line receiver's power consumption is greatest.

11 Claims, 4 Drawing Sheets





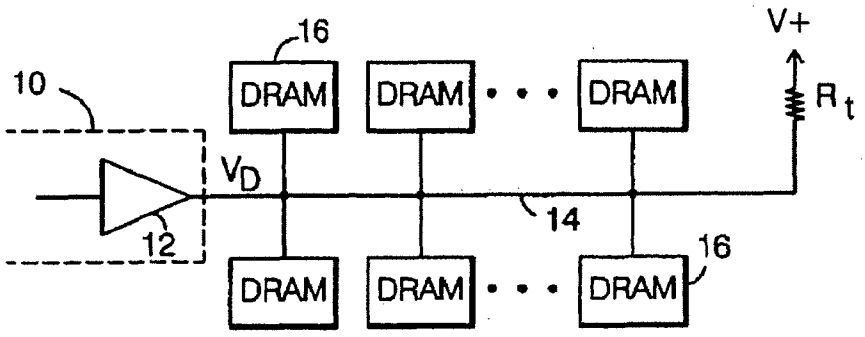


FIG.1a
(Prior Art)

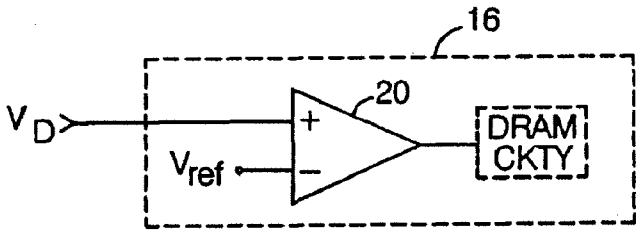


FIG.1b
(Prior Art)

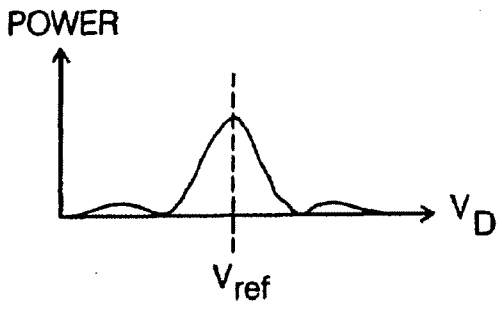


FIG.1c

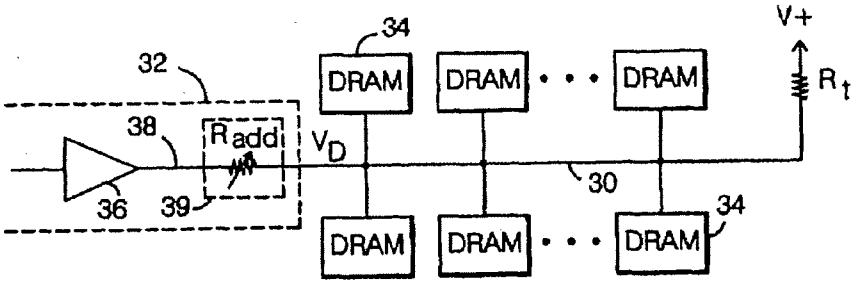
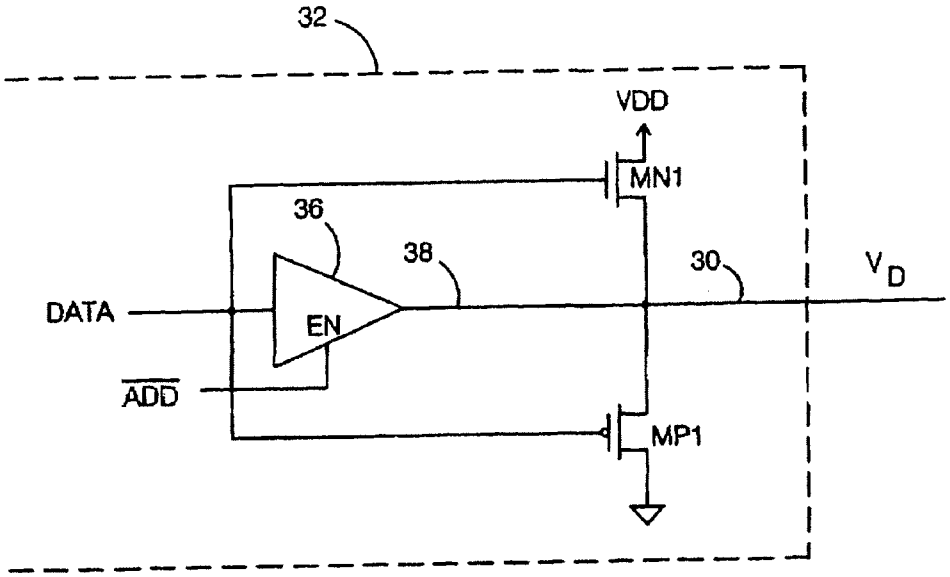

32
34
DRAM
DRAM
DRAM
V+
R_t
38
R_{add}
V_D
30
36
39
DRAM
DRAM
DRAM
34

FIG.2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VDD
MN1
36
38
30
V_D
DATA
EN
ADD
MP1

FIG.6

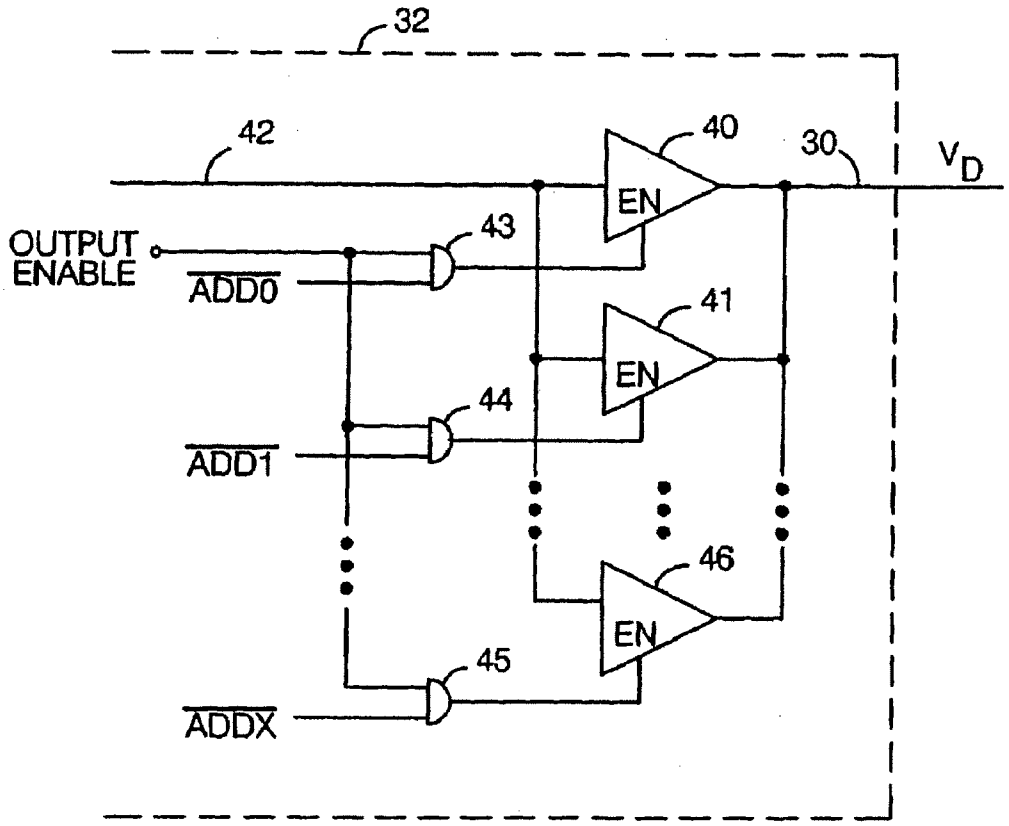

32
42
40
30
V_D
EN
OUTPUT ENABLE
43
ADD0
41
EN
44
ADD1
46
EN
45
ADDX

FIG.3

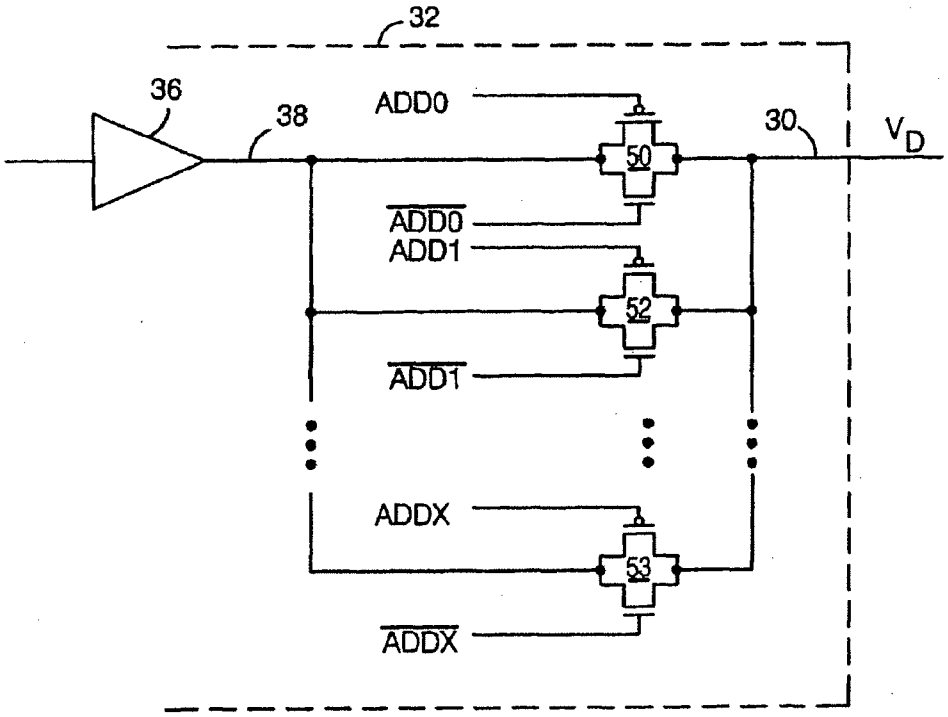

32
36
38
ADD0
30
V_D
50
$\overline{ADD0}$
ADD1
52
$\overline{ADD1}$
ADDX
53
$\overline{ADDX}$

FIG.4

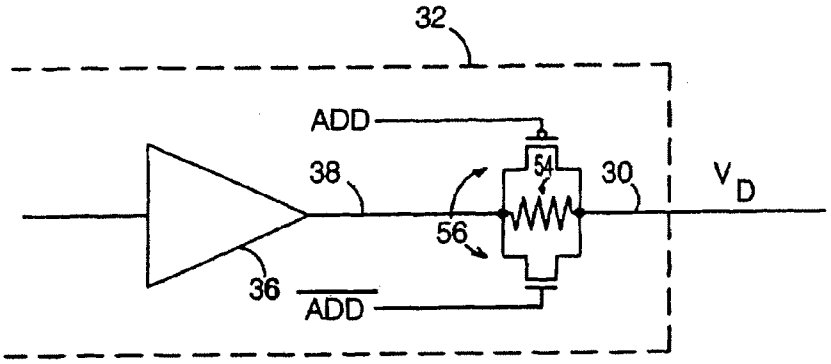

32
ADD
38
54
30
V_D
56
36
$\overline{ADD}$

FIG.5

OUTPUT BUFFER WITH SWITCHABLE OUTPUT IMPEDANCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of output buffers, and particularly to output buffers used to drive terminated signal lines.

2. Description of the Related Art

There are many applications in which output buffers drive respective signal lines to convey data to one or more devices connected to the signal lines. In such applications, it is important that the integrity of the data on the signal lines be maintained, so that it can be accurately detected by the receiving devices.

One such application is a random access memory (RAM) system. Dual-Inline Memory Modules (DIMMs) are the industry-standard platform on which RAM is provided for digital computers. Each DIMM is a printed-circuit board which contains a number of individual RAM integrated circuits (ICs) or "chips." DIMMs typically contain address and/or control registers which distribute data bits to each of the DIMM's RAM chips via signal lines driven by respective output buffers.

A typical DIMM arrangement is shown in FIG. **1***a*. An output buffer **10** includes a drive circuit **12** which drives a signal line **14**. The DIMM includes a number of RAM chips **16**; dynamic RAM (DRAM) chips are shown in FIG. **1**, though a DIMM can include other RAM types as well. Signal line **14** is routed to an address or control input on each RAM chip.

DIMMs are provided in a variety of configurations. Each DIMM type has an associated set of specifications, promulgated by the industry-supported JEDEC Solid State Technology Association international standards body, which govern the DIMM's configuration and operation. For some DIMM types, the specifications require that each signal line be "terminated"; i.e., that a termination resistor R_t be connected between each signal line and a fixed voltage, denoted in FIG. **1** as V+. Termination resistors serve to improve the signal quality on transmission lines such as signal line **14**.

The use of termination resistors in this way can have an undesirable side effect, however, in that they tend to increase the DIMM's power consumption. For example, assuming that the output impedance of drive circuit **12** is ~0 Ω, V+ is 0.75 volts, and R_t is 30 Ω, then the static power dissipation P_{diss} associated with one signal line is:

$P_{diss}=(V+)^2/R_t=18.75$ mW/signal line. There are typically 20-30 signal lines on a DIMM, such that power dissipation due to R_t can be 500 mW or more.

One approach which has been suggested to reduce P_{diss} is to make the output of drive circuit **12** a 'tri-state' output, which presents a high impedance to signal line **14** during a low power or 'standby' mode. This reduces the voltage across R_t to zero, and thus P_{diss} is also reduced to zero. However, this solution may give rise to another problem, which is illustrated in FIGS. **1***b* and **1***c*. Signals provided to a DRAM input are typically received by a line receiver **20**, which determines the logic state of the signal line by comparing the signal line voltage (V_D) with a reference voltage (V_{ref}). As shown in FIG. **1***c*, the power consumed by line receiver **20** is greatest when V_D is equal to V_{ref}, and decreases as the difference between V_D and V_{ref} increases. V_{ref} is typically made equal to one-half of the memory system's supply voltage, which is also a preferred voltage for V+. When V_{ref}=V+, enabling the 'standby' mode causes V_D to be pulled up to V_{ref} via termination resistor R_t. This causes the power consumption of each DRAM line receiver to spike, resulting in a total power consumption which may be unacceptably high.

SUMMARY OF THE INVENTION

An output buffer with a switchable output impedance is presented which overcomes the problems noted above, by reducing power dissipation that would otherwise arise due the termination resistor on a signal line being driven, as well as avoiding undesirable power consumption by signal line receivers such as those found in DRAM chips.

The present output buffer is designed for driving a terminated signal line. The buffer includes a drive circuit, and a means for switching the output impedance of the drive circuit between a relatively low value—typically <20 Ω—when the output buffer is operated in a first, 'normal' mode, and a value greater than the 'normal' value when the output buffer is operated in a second mode such as a low power or 'standby' mode. By increasing the drive circuit's output impedance while in 'standby' mode, power dissipation due to the termination resistor is reduced. Several means for controlling the drive circuit's output impedance are described.

The present output buffer may be advantageously employed in any application for which terminated signal lines need to be driven. The buffer can be particular useful when used in a memory system as described above, such as a DDR3 memory system having signal lines terminated in accordance with applicable JEDEC specifications. In this application, additional power savings may be realized by arranging the buffer such that the increased impedance in low power mode shifts the signal line voltage so as to avoid the voltage range over which a line receiver's power consumption is greatest. When so arranged, a memory system's total power consumption can be significantly reduced.

Further features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1***a* is a block diagram of a known memory system configuration.

FIG. **1***b* is a block diagram depicting a DRAM chip which includes a line receiver.

FIG. **1***c* is a graph plotting line voltage versus power consumption for the line receiver of FIG. **1***b*.

FIG. **2** is a block diagram of an output buffer per the present invention, as it might be employed in a memory system application.

FIG. **3** is a schematic diagram of one possible implementation of an output buffer per the present invention.

FIG. **4** is a schematic diagram of another possible implementation of an output buffer per the present invention.

FIG. **5** is a schematic diagram of another possible implementation of an output buffer per the present invention.

FIG. **6** is a schematic diagram of another possible implementation of an output buffer per the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present output buffer with switchable output impedance is intended for use driving terminated signal lines, particularly when power consumption is a concern. By controlling the buffer's output impedance, the power consumption of a system employing the buffer can be reduced in comparison with systems which lack this capability.

Though the present buffer is generally applicable to any terminated signal line application, a primary application is in a memory system, in which each buffer drives a respective terminated address or control line routed to multiple RAM chips populating a DIMM memory module. For example, for DIMMs in compliance with the DDR3 specifications promulgated by JEDEC, each address and control line is routed to multiple DRAM chips on the DIMM, and each line is terminated with a termination resistor having a resistance R_t. For purposes of illustration, this application is described throughout, though the invention is in no way limited to use with DIMMs.

The basic principles of an output buffer per the present invention are illustrated in FIG. **2**. A signal line **30** is terminated with a termination resistor having a resistance R_t, which is connected between the signal line and a fixed voltage V+. Signal line **30** is driven by an output buffer **32**; in a DIMM application as described above, output buffer **32** conveys data bits to an input of each RAM chip **34** on the DIMM via signal line **30**.

Output buffer **32** includes a drive circuit **36** which produces an output **38**. Buffer **32** also includes a means for switching the output impedance of drive circuit **36** between at least two values. Typically, the buffer is arranged such that the output impedance is switchable between a relatively low impedance (typically <20Ω) when the buffer is operated in a first, 'normal' mode, and an output impedance which is greater than the 'normal' mode value when the buffer is operated in a second, 'standby' mode. The switchable impedance (**39**) is represented in FIG. **2** with a variable resistance R_{add} connected in series with the output of drive circuit **36**, though means other than a series resistance might also be used, as discussed below. Note that, in 'standby' mode, the drive circuit output need not go into a 'tri-state' mode as in the prior art. By making the drive circuit's output impedance switchable as described herein, the drive circuit output may remain at a logic '0' or logic '1' state in 'standby' mode.

Increasing the impedance of the drive circuit output reduces the power dissipation that arises due to the termination resistor. When R_{add}=0, static power dissipation P_{diss} is given by:

$$P_{diss}=(V+)^2/R_t$$

Assuming R_t=30Ω and V+=0.75 volts,

$P_{diss}=(V+)^2/R_t$=18.75 mW/signal line. There are typically 20-30 signal lines on a DIMM, such that P_{diss} due to R_t can be 500 mW or more.

However, when R_{add} is increased to, for example, 100Ω, the equation for P_{diss} becomes:

$P_{diss}=(V+)^2/(R_t+R_{add})$=4.33 mW/signal line. Thus, switching the output impedance of buffer **32** from ~0Ω to ~100Ω reduces static power dissipation to about one-fourth its previous value.

The increase in the drive circuit's output impedance in 'standby' mode also serves to shift the signal line voltage (V_D). Using the values for V+, R_{add} and R_t from the example above, during 'standby' mode, the signal line voltage V_D is given by:

$$V_D=(V+*R_{add})/(R_{add}+R_t)\sim 0.58 \text{ volts.}$$

If V_D is received by line receivers as shown in FIGS. **1***b* and **1***c*, the increased output impedance ideally shifts V_D out of the range over which the line receiver's power consumption is greatest, thereby resulting in a further reduction in power dissipation. The non-zero value of R_{add} should be chosen such that, when the drive circuit output is a logic '0', V_D is low enough so that the power consumed by the line receivers coupled to the driven signal line is near zero; similarly, if the drive circuit output is a logic '1', V_D should be high enough to avoid the voltage range for which the line receivers' power consumption is greatest. This can be achieved by choosing a small value for R_{add}. However, as shown above, the smaller the value of R_{add} the larger the static power dissipation in the termination. Hence, a suitable median value needs to be chosen for R_{add}, based on system characteristics like line receiver power dissipation vs. signal line voltage, termination value, supply voltage and desired power savings.

The output impedance of drive circuit **36** may be made switchable by a wide variety of means. Several possible exemplary implementations are described below; however, other means by which the output impedance can be switched between a relatively low first value and at least one other value which is greater than the first value may also be acceptable.

One possible implementation for an output buffer per the present invention is shown in FIG. **3**. Here, output buffer **32** contains at least two drive circuits (**40**, **41**) connected in parallel. Each drive circuit receives the same input signal (**42**), and their outputs are tied together to provide a common output which drives signal line **30**. The drive circuits are preferably activated in response to an "enable" signal (EN). In this approach, the overall output impedance for buffer **32** varies with the number of active drive circuits connected in parallel, with output impedance decreasing as more drive circuits are activated.

For the exemplary embodiment shown in FIG. **3**, the output impedance is controlled by enabling a desired number of drive circuits. The output buffer would typically receive an "output enable" signal, which is logically combined with respective independent control signals ($\overline{\text{ADD0}}$, $\overline{\text{ADD1}}$)—here, using AND gates **43** and **44**—to provide enable signals to respective driver circuits. Additional resolution for setting the buffer's output impedance could be obtained by connecting additional drive circuits (**46**) in parallel with drive circuits **40** and **41** and providing control signals ($\overline{\text{ADDX}}$ via AND gate **45**) to their enable inputs as needed to achieve a desired output impedance. As the number of active parallel drive circuits (**40**,**41**,**46**) is increased, the output impedance decreases. A tri-state mode could be enabled by setting the "output enable" signal so that all the drive circuits are off.

Another possible implementation for an output buffer **32** per the present invention is shown in FIG. **4**. Here, the means for switching the buffer's output impedance comprises at least two pass gates (**50**, **52**) connected in parallel, with each pass gate input connected to receive the output **38** of drive circuit **36**, and each pass gate output connected together to drive signal output line **30**. When so arranged, the overall output impedance for buffer **32** varies with the number of 'on' pass gates, with output impedance decreasing as more pass gates are turned on. Each pass gate is controlled with a respective pair of control signals (ADD0, $\overline{\text{ADD0}}$; ADD1, $\overline{\text{ADD1}}$). Additional output impedance values could be achieved by connecting additional pass gates (**53**) in parallel with pass gates **50** and **52** and providing control signals (ADDX, $\overline{\text{ADDX}}$) to turn them on or off as needed to achieve a desired output impedance. A tri-state mode could be enabled by setting the control signals so that all the pass gates are off.

Another possible embodiment is shown in FIG. **5**. Here, a resistance **54** is connected in series with the output of drive circuit **36**, and a switch is connected across the resistance. In FIG. **5**, the switch is implemented with a pass gate **56**, though

other switch types could also be used. The resistance itself could be implemented by using a physical resistor or using transistors.

In 'normal' mode, the switch is closed, so that resistance **54** is effectively bypassed and the drive circuit's output impedance is relatively low. In 'standby' mode, the switch across resistance **54** is switched off, increasing the output impedance by an amount approximately equal to the value of resistance **54**.

Further tunability of the output impedance could be achieved by connecting multiple switch/resistance pairs in series with the output of drive circuit **36**, with each switch being independently controllable. Multiple pass gates could be used to realize such an implementation; note, however, that each pass gate adds capacitance which slows down the output signal.

Yet another possible implementation for an output buffer **32** per the present invention is shown in FIG. **6**. Here, the means for switching the buffer's output impedance comprises an NMOS FET MN1 connected between the system's positive supply voltage V_{DD} and signal output line **30**, and a PMOS FET MP1 connected between the signal output line and circuit ground. The FETs are operated so as to effectively increase the output buffer's output impedance and to shift the signal line voltage during 'standby' mode. When implemented as shown in FIG. **6**, during 'standby' mode ($\overline{ADD}$='low'), drive circuit **36** is disabled. If the data bit (DATA) is 'high', MP1 is turned off, and MN1 is turned on and pulls signal line **30** to a voltage given by V_{DD}-V_{th}, where V_{th} is MN1's threshold voltage; MN1 presents a high output impedance to signal line **30**. If DATA is 'low', MN1 is turned off, and MP1 is turned on and pulls signal line **30** to a voltage given by V_{th}, where V_{th} is MP1's threshold voltage, again presenting a high output impedance to signal line **30**.

Note that the methods shown in FIGS. **3**, **4**, **5** and **6** for controlling the output impedance switching means are merely exemplary. There are myriad ways in which these circuits could be realized, and many possible control schemes for operating them. It is only essential that the present output buffer include a drive circuit having an output adapted to drive a terminated signal line, and a means for switching the output impedance of the drive circuit between a relatively low 'normal' output impedance and a higher 'standby' output impedance, so as to reduce the power dissipation of the output buffer when operated in 'standby' mode.

Note that, though the schematics contained herein depict the use of field-effect transistors (FETs), bipolar transistors or other state-of-the-art current switching integrated circuit devices could also be used.

While particular embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

We claim:

1. An output buffer, comprising:

a first drive circuit having an output adapted to drive a signal line terminated with a termination resistor; and

a means for switching the output impedance of said first drive circuit between a first, relatively low output impedance when said output buffer is operated in a first mode and a second output impedance which is greater than said first output impedance when said output buffer is operated in a second mode, so as to reduce the power dissipation in said termination resistor when said output buffer is operated in said second mode;

wherein said output buffer is connected between and powered by first supply voltage VDD and a second supply voltage, said means for switching the output impedance of said drive circuit comprising:

an n-type transistor connected between V_{DD} and said output; and

a p-type transistor connected between said output and said second supply voltage;

said buffer arranged to operate said transistors so as to increase the effective output impedance of said drive circuit when said output buffer is operated in said second mode.

2. The output buffer of claim **1**, wherein said output buffer buffers a data bit received at an input, said output buffer arranged such that, when operated in said second mode, said p-type transistor is turned off and said n-type transistor is turned on when said data bit is 'high' such that said output is pulled to a voltage given by V_{DD}-V_{th}, and said n-type transistor is turned off and said p-type transistor is turned on when said data bit is 'low' such that said output is pulled to V_{th}.

3. The output buffer of claim **2**, wherein said output buffer is arranged such that it is disabled when operated in said second mode.

4. An output buffer, comprising:

a first drive circuit having an output adapted to drive a signal line terminated with a termination resistor; and

a means for switching the output impedance of said first drive circuit between a first, relatively low output impedance when said output buffer is operated in a first mode and a second output impedance which is greater than said first output impedance when said output buffer is operated in a second mode, so as to reduce the power dissipation in said termination resistor when said output buffer is operated in said second mode;

wherein said output buffer is contained within an address register which contains a plurality of said output buffers, said buffers arranged to provide respective output signals which drive respective signal lines, at least some of which are connected to the address or control inputs of respective random-access memory (RAM) chips residing on a Dual-Inline Memory Module (DIMM), and

wherein said RAM chips include respective receivers for each of said address or control inputs, each of said receivers coupled to a respective one of said signal lines and having an associated power consumption which is greatest when the voltage on said signal line is within a known range, said means for switching the output impedance of said drive circuit arranged to ensure that the voltage on said signal line is outside of said known range when said output buffer is operated in said second mode.

5. The output buffer of claim **4**, wherein said second output impedance is selected such that, when said output buffer is operated in said second mode, the voltage on said signal line is below said known range when said buffer's output is 'low'and such that the voltage on said signal line is above said known range when said buffer's output is 'high'.

6. An output buffer, comprising:

a first drive circuit having an output adapted to drive a signal line terminated with a termination resistor; and

a means for switching the output impedance of said first drive circuit between a first, relatively low output impedance when said output buffer is operated in a first mode and a second output impedance which is greater than said first output impedance when said output buffer is operated in a second mode, so as to reduce the power

dissipation in said termination resistor when said output buffer is operated in said second mode;

wherein said means for switching the output impedance of said first drive circuit comprises:

a first switch/resistance pair, comprising:

a resistance which is connected in series with said drive circuit output; and

a switch connected across said resistance which is opened and closed in response to a control signal, said switch closed in said first mode such that a relatively low output impedance is presented to said signal line, and said switch opened in said second mode such that an output impedance approximately equal to said resistance is presented to said signal line.

7. The output buffer of claim 6, wherein said switch is a pass gate.

8. The output buffer of claim 6, wherein said means for switching the output impedance comprises at least one additional switch/resistance pair connected in series with said first switch/resistance pair, said switches opened and closed in response to respective control signals to present a desired output impedance to said signal line.

9. A memory system, comprising:

a plurality of signal lines which route signals from respective output buffers to the address or control inputs of a plurality of random-access memory (RAM) chips residing on a Dual-Inline Memory Module (DIMM), said RAM chips including respective receivers for each of said address or control inputs, each of said receivers coupled to a respective one of said signal lines and having an associated power consumption which is greatest when the voltage on said signal line is within a known range; and

a plurality of termination resistors connected between a fixed voltage and respective ones of said signal lines to terminate said signal lines;

each of said output buffers comprising:

a drive circuit having an output connected to drive a respective one of said terminated signal lines; and

a means for switching the output impedance of said drive circuit between a first, relatively low output impedance when said output buffer is operated in a first mode and a second output impedance which is greater than said first output impedance when said output buffer is operated in a second mode so as to reduce the power dissipation in said termination resistor and to ensure that the voltage on said signal line is outside of said known range when said output buffer is operated in said second mode.

10. The memory system of claim 9, wherein said DIMM is part of a DDR3 memory system, said signal lines terminated in accordance with applicable JEDEC specifications.

11. The memory system of claim 9, wherein said means for switching the output impedance of said drive circuit comprises a resistance which is connected in series with said drive circuit output in response to at least one control signal.

* * * * *

EXHIBIT C

NETLIST Powering the Future of Information Technology

Print this page

HyperCloud™ Memory

Flash Memory

DRAM Memory Modules

SDRAM

DDR

DDR2

DDR3
> DDR3 SO-DIMM
> DDR3 UDIMM
> DDR3 RDIMM

Testing Tools

DDR3 RDIMM

Netlist DDR3 (Double Data Rate 3) Registered Dual In-Line Memory Modules (RDIMMs) are designed to deliver unprecedented performance and energy efficiency required by space constrained, high-end servers, blades and workstations. This solution offers greatly improved power savings to increase the overall thermal characteristics of servers, maximizes the amount of memory in the system while keeping slots open for future upgrades.

DDR3-800 240-pin Registered DIMM

Height	Module Description	Netlist P/N #	Device	Density	Package
1.18	1GB, 128MX72, 1 Rank	NLD127R31207H-D64x	128MX8	1024	CSP
1.18	2GB, 256MX72, 2 Rank	NLD257R31207H-D64x	128MX8	1024	CSP
1.18	4GB, 512MX72, 2 Rank	NLD517R32503H-D64x	256Mx4	1024	CSP

DDR3-800 240-pin Registered DIMM w/Thermal Sensor

Height	Module Description	Netlist P/N #	Device	Density	Package
1.18	1GB, 128MX72, 1 Rank	NLD127T31207H-D64x	128MX8	1024	CSP
1.18	2GB, 256MX72, 2 Rank	NLD257T31207H-D64x	128MX8	1024	CSP
1.18	4GB, 512MX72, 2 Rank	NLD517T32503H-D64x	256Mx4	1024	CSP

DDR3-1067 240-pin Registered DIMM

Height	Module Description	Netlist P/N #	Device	Density	Package
1.18	1GB, 128MX72, 1 Rank	NLD127R31207H-D85x	128MX8	1024	CSP
1.18	2GB, 256MX72, 2 Rank	NLD257R31207H-D85x	128MX8	1024	CSP
1.18	4GB, 256MX72, 2 Rank	NLD257R31203H-D85x	256Mx4	1024	CSP

DDR3-1067 240-pin Registered DIMM w/Thermal Sensor

Height	Module Description	Netlist P/N #	Device	Density	Package
1.18	1GB, 128MX72, 1 Rank	NLD127T31207H-D85x	128MX8	1024	CSP
1.18	2GB, 256MX72, 2 Rank	NLD257T31207H-D85x	128MX8	1024	CSP
1.18	4GB, 256MX72, 2 Rank	NLD517T32503H-D85x	256Mx4	1024	CSP

How to Order

For additional information, call us at (949) 679-0100 or email info@netlist.com

EXHIBIT D

NETLIST

HyperCloud™ 16GB 2 vRank DDR3 RDIMM

Product Brief

Netlist introduces HyperCloud™ memory technology that enables 384 GigaBytes (GB) of DRAM to be populated in a dual socket server. This achievement makes possible unprecedented server performance for datacenter applications.

Breaking the Memory Barrier with Rank Multiplication

This advanced technology breaks the 192GB memory-barrier in dual socket servers. The new DDR3 RDIMM presents two virtual ranks (vRanks) to the Memory Controller Hub (MCH), allowing four 16GB 2 vRank DIMMs per channel. Using Netlist's patented rank multiplication technology, 16GB two virtual rank (four physical ranks) RDIMMs can fully populate a dual socket server with 288GB of memory (up to 384GB in 24 slot systems).

Maximum Data-Rate with Load Reduction

In addition, the HyperCloud memory rank multiplication implements load reduction for higher data speeds. Servers populated with four DIMMs per channel can operate at the maximum data-rate of 1333MT/s providing maximum memory bandwidth and increased server performance.

Datacenter Savings with Server Optimization

Servers are typically underutilized due to memory bottlenecks. HyperCloud memory solves this problem by offering the highest DRAM capacity and memory bandwidth possible which maximizes server utilitization and increases computational power. Optimal server utilization is especially important in server virtualization, memcache, database, and high performance computing applications.

Features

- 4GB, 8GB, 16GB 2 vRank module options
- Rank multiplication
- Load reduction
- Increases DRAM server capacity up to 384GB
- Supports 4 DIMMS per channel at 1333MT/s
- RoHS 6/6
- JEDEC compatible

Benefits

- Increases server performance
- Provides lower power
- Reduces TCO
- Lowers memory costs

Applications

- Virtualization
- Search
- Cloud computing
- High performance computing
- Video services
- Memcache appliances
- Online gaming

HyperCloud™ 16GB 2 vRank DDR3 RDIMM

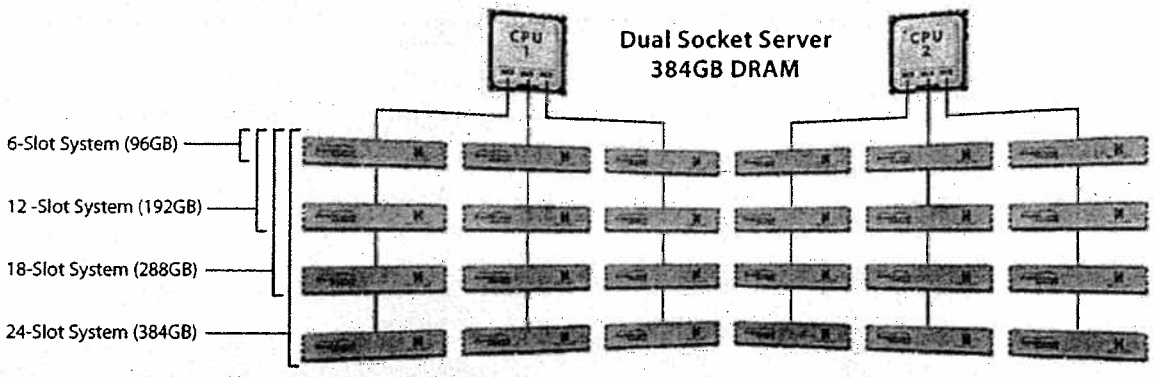
Optimal DRAM Server Capacity with HyperCloud Technology

Netlist HyperCloud memory allows one, two, three or four DIMMs per channel to be populated with the maximum density and highest memory bandwidth vs standard JEDEC RDIMMs. HyperCloud rank multiplication technology presents two virtual ranks (four physical ranks) or one virtual rank (two physical ranks) to the Memory Controller Hub (MCH).

Speed	Physical Rank	Virtual Rank[1]	2 DIMMs Populated		3 DIMMs Populated		4 DIMMs Populated	
			Standard	Netlist	Standard	Netlist	Standard	Netlist
DDR3-800	2R	–	JEDEC	JEDEC	JEDEC	JEDEC	JEDEC	JEDEC
	4R	2R	JEDEC	JEDEC	N/A	HyperCloud	N/A	HyperCloud
DDR3-1066	2R	1R	JEDEC	JEDEC	N/A	HyperCloud	N/A	HyperCloud
	4R	2R	N/A	HyperCloud	N/A	HyperCloud	N/A	HyperCloud
DDR3-1333	2R	1R	N/A	HyperCloud	N/A	HyperCloud	N/A	HyperCloud
	4R	2R	N/A	HyperCloud	N/A	HyperCloud	N/A	HyperCloud

[1] Applies to HyperCloud.

DRAM capacities of 96GB, 192GB, 288GB, and up to 384GB per dual socket server are possible utilizing 16GB 2 vRank HyperCloud RDIMMs.



Product Description	Form Factor	Ordering Number
4GB 1333MHz 2Rx8 (1Gb) DDR3	Planar LP	NMD517G31207HD10
8GB 1333MHz 2Rx8 (2Gb) DDR3	Planar LP	NMD1G7G32507HD10
8GB 1333MHz 2Rx4 (1Gb) DDR3	Planar-X LP	NMD1G7G3250DHD10
16GB 1333MHz 2Rx4 (2Gb) DDR3	Planar-X LP	NMD2G7G3510DHD10

NETLIST

JEDEC QMS RoHS

Corporate Headquarters
Netlist, Inc.
51 Discovery
Irvine, CA 92618
www.netlist.com
949-679-0100
sales@netlist.com

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

NOTICE OF ASSIGNMENT TO UNITED STATES MAGISTRATE JUDGE FOR DISCOVERY

This case has been assigned to District Judge Ronald S. W. Lew and the assigned discovery Magistrate Judge is Carla Woehrle.

The case number on all documents filed with the Court should read as follows:

CV09- 8749 RSWL (CWx)

Pursuant to General Order 05-07 of the United States District Court for the Central District of California, the Magistrate Judge has been designated to hear discovery related motions.

All discovery related motions should be noticed on the calendar of the Magistrate Judge

---

NOTICE TO COUNSEL

A copy of this notice must be served with the summons and complaint on all defendants (if a removal action is filed, a copy of this notice must be served on all plaintiffs).

Subsequent documents must be filed at the following location:

[X] **Western Division** **312 N. Spring St., Rm. G-8** **Los Angeles, CA 90012**	[ ] **Southern Division** **411 West Fourth St., Rm. 1-053** **Santa Ana, CA 92701-4516**	[ ] **Eastern Division** **3470 Twelfth St., Rm. 134** **Riverside, CA 92501**

Failure to file at the proper location will result in your documents being returned to you.

RICHARD H. ZAITLEN #63283
CAROLYN S. LU #233825
PILLSBURY WINTHROP SHAW PITTMAN LLP
725 S. Figueroa Street, Suite 2800
Los Angeles, CA 90017-5406
Telephone: (213) 488-7100
Facsimile: (213) 629-1033
Attorneys for Plaintiff INPHI CORPORATION

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

INPHI CORPORATION, A Delaware Corporation, PLAINTIFF(S) v.	CASE NUMBER CV09-8749 RSWL (CWx)
NETLIST, INC., A Delaware Corporation, DEFENDANT(S).	**SUMMONS**

TO:DEFENDANT(S): NETLIST, INC., A Delaware Corporation

A lawsuit has been filed against you.

Within 20 days after service of this summons on you (not counting the day you received it), you must serve on the plaintiff an answer to the attached ☒ complaint ☐ _____ amended complaint ☐ counterclaim ☐ cross-claim or a motion under Rule 12 of the Federal Rules of Civil Procedure. The answer or motion must be served on the plaintiff's attorney, Richard H. Zaitlen/Carolyn S. Lu, whose address is Pillsbury Winthrop Shaw Pittman LLP, 725 S. Figueroa St., Suite 2800, Los Angeles, CA 90017-5406. If you fail to do so, judgment by default will be entered against you for the relief demanded in the complaint. You also must file your answer or motion with the court.

Clerk, U.S. District Court

Dated: 30 NOV 2009

By: SHEA BOURGEOIS
Deputy Clerk

(Seal of the Court) SEAL

[Use 60 days if the defendant is the United States or a United States agency, or is an officer or employee of the United States. Allowed 60 days by Rule 12(a)(3)].

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

I (a) PLAINTIFFS (Check box if you are representing yourself ☐)
INPHI CORPORATION, A Delaware Corporation,

DEFENDANTS
NETLIST, INC., A Delaware Corporation,

(b) Attorneys (Firm Name, Address and Telephone Number. If you are representing yourself, provide same.)
RICHARD H. ZAITLEN #63283 Tel: (213) 488-7100
CAROLYN S. LU #233825
PILLSBURY WINTHROP SHAW PITTMAN LLP
725 S. Figueroa Street, Suite 2800
Los Angeles, CA 90017-5406

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an X in one box only.)

☐ 1 U.S. Government Plaintiff
☒ 3 Federal Question (U.S. Government Not a Party
☐ 2 U.S. Government Defendant
☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES - For Diversity Cases Only
(Place an X in one box for plaintiff and one for defendant.)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated or Principal Place of Business in this State	☒ 4	☒ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated and Principal Place of Business in Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. ORIGIN (Place an X in one box only.)

☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify): ☐ 6 Multi-District Litigation ☐ 7 Appeal to District Judge from Magistrate Judge

V. REQUESTED IN COMPLAINT: JURY DEMAND: ☒ Yes ☐ No (Check 'Yes' only if demanded in complaint.)

CLASS ACTION under F.R.C.P. 23: ☐ Yes ☒ No ☒ **MONEY DEMANDED IN COMPLAINT: $** Unspecified

VI. CAUSE OF ACTION (Cite the U. S. Civil Statute under which you are filing and write a brief statement of cause. Do not cite jurisdictional statutes unless diversity.)
35 U.S. Section 271 Patent Infringement

VII. NATURE OF SUIT (Place an X in one box only.)

OTHER STATUTES
☐ 400 State Reapportionment
☐ 410 Antitrust
☐ 430 Banks and Banking
☐ 450 Commerce/ICC Rates/etc.
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☐ 480 Consumer Credit
☐ 490 Cable/Sat TV
☐ 810 Selective Service
☐ 850 Securities/Commodities/ Exchange
☐ 875 Customer Challenge 12 USC 3410
☐ 890 Other Statutory Actions
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☐ 900 Appeal of Fee Determination Under Equal Access to Justice
☐ 950 Constitutionality of State Statutes

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☐ 220 Foreclosure
☐ 230 Rent Lease & Ejectment
☐ 240 Torts to Land
☐ 245 Tort Product Liability
☐ 290 All Other Real Property

TORTS PERSONAL INJURY
☐ 310 Airplane
☐ 315 Airplane Product Liability
☐ 320 Assault, Libel & Slander
☐ 330 Fed. Employers' Liability
☐ 340 Marine
☐ 345 Marine Product Liability
☐ 350 Motor Vehicle
☐ 355 Motor Vehicle Product Liability
☐ 360 Other Personal Injury
☐ 362 Personal Injury-Med Malpractice
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☐ 650 Airline Regs
☐ 660 Occupational Safety /Health
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LABOR
☐ 710 Fair Labor Standards Act
☐ 720 Labor/Mgmt. Relations
☐ 730 Labor/Mgmt. Reporting & Disclosure Act
☐ 740 Railway Labor Act
☐ 790 Other Labor Litigation
☐ 791 Empl. Ret. Inc. Security Act

PROPERTY RIGHTS
☐ 820 Copyrights
☒ 830 Patent
☐ 840 Trademark

SOCIAL SECURITY
☐ 61 HIA(1395ff)
☐ 862 Black Lung (923)
☐ 863 DIWC/DIWW 405(g))
☐ 864 SSID Title XVI
☐ 865 RSI (405(g))

FEDERAL TAX SUITS
☐ 870 Taxes (U.S. Plaintiff or Defendant)
☐ 871 IRS-Third Party 26 USC 7609

CV09-8749

FOR OFFICE USE ONLY: Case Number: _____

AFTER COMPLETING THE FRONT SIDE OF FORM CV-71, COMPLETE THE INFORMATION REQUESTED BELOW.

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

VIII(a). IDENTICAL CASES: Has this action been previously filed in this court and dismissed, remanded or closed? ☒ No ☐ Yes
If yes, list case number(s): _____

VIII(b). RELATED CASES: Have any cases been previously filed in this court that are related to the present case? ☒ No ☐ Yes
If yes, list case number(s): _____

Civil cases are deemed related if a previously filed case and the present case:

(Check all boxes that apply)
- ☐ A. Arise from the same or closely related transactions, happenings, or events; or
- ☐ B. Call for determination of the same or substantially related or similar questions of law and fact; or
- ☐ C. For other reasons would entail substantial duplication of labor if heard by different judges; or
- ☐ D. Involve the same patent, trademark or copyright, and one of the factors identified above in a, b or c also is present.

IX. VENUE: (When completing the following information, use an additional sheet if necessary.)

(a) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named plaintiff resides.
☐ Check here if the government, its agencies or employees is a named plaintiff. If this box is checked, go to item (b).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Los Angeles County	

(b) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named defendant resides.
☐ Check here if the government, its agencies or employees is a named defendant. If this box is checked, go to item (c).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Orange County	

(c) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** claim arose.
Note: In land condemnation cases, use the location of the tract of land involved.

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Los Angeles County	

*** Los Angeles, Orange, San Bernardino, Riverside, Ventura, Santa Barbara, or San Luis Obispo Counties**
Note: In land condemnation cases, use the location of the tract of land involved

X. SIGNATURE OF ATTORNEY (OR PRO PER): _____ **Date** November 30, 2009

Notice to Counsel/Parties: The CV-71 (JS-44) Civil Cover Sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law. This form, approved by the Judicial Conference of the United States in September 1974, is required pursuant to Local Rule 3 -1 is not filed but is used by the Clerk of the Court for the purpose of statistics, venue and initiating the civil docket sheet. (For more detailed instructions, see separate instructions sheet.)

Key to Statistical codes relating to Social Security Cases:

Nature of Suit Code	Abbreviation	Substantive Statement of Cause of Action
861	HIA	All claims for health insurance benefits (Medicare) under Title 18, Part A, of the Social Security Act, as amended. Also, include claims by hospitals, skilled nursing facilities, etc., for certification as providers of services under the program. (42 U.S.C. 1935FF(b))
862	BL	All claims for "Black Lung" benefits under Title 4, Part B, of the Federal Coal Mine Health and Safety Act of 1969. (30 U.S.C. 923)
863	DIWC	All claims filed by insured workers for disability insurance benefits under Title 2 of the Social Security Act, as amended; plus all claims filed for child's insurance benefits based on disability. (42 U.S.C. 405(g))
863	DIWW	All claims filed for widows or widowers insurance benefits based on disability under Title 2 of the Social Security Act, as amended. (42 U.S.C. 405(g))
864	SSID	All claims for supplemental security income payments based upon disability filed under Title 16 of the Social Security Act, as amended.
865	RSI	All claims for retirement (old age) and survivors benefits under Title 2 of the Social Security Act, as amended. (42 U.S.C. (g))